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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/992,121	HILTON, RONALD	
	Examiner	Art Unit	
	David Silver	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 3-14 are currently pending in Instant Application.

2. The Instant Application is not currently in condition for allowance.

Priority

3. Claimed priority has been acknowledged in previous Office Action **(Effective Filing: 11/14/2001)**.

Response to Arguments

Response: Claim Interpretation

4. Applicants' statements in Remarks filed 5/14/07 section 10 have been fully noted. It is believed that the claim interpretation is wholly consistent with MPEP 2111.04. Applicants' arguments are not persuasive for the reasons previously provided. MPEP 2111.04 recites, in part: "Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed, or by claim language that does not limit a claim to a particular structure.".
The mere ability, enablement, or adaptability to perform a function does not necessitate the performance of such function or its use. Therefore, if a limitation does not necessitate the performance of the function, an art that does not expressly prohibit the performance of the function anticipates the claim scope. This interpretation is support by MPEP 2111.04 [R-3], which recites in part:

> "Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed, or by claim language that does not limit a claim to a particular structure. However, examples of claim language, although not exhaustive, that may raise a question as to the limiting effect of the language in a claim are: (A)"adapted to" or "adapted for" clauses; (B)"wherein" clauses; and (C)"whereby" clauses." (MPEP 2111.04)

Response: 35 U.S.C. § 101

5. **Applicants argue:**

"20.4. The method claimed is for "dynamic emulation of legacy instructions" and the method is implemented in a computer. Anyone skilled in the art would immediately recognize that such a computer-implemented "dynamic emulation of legacy instructions" produces "a useful, tangible, and concrete final result". The final result is "emulation of legacy instructions" and no one can reasonably question that

such a result is both "tangible" and "useful".

20.5. The Examiner appears to argue that most all "software algorithms" (that is, the ones that do not provide a physical transformation) in a computer do not produce a "tangible result" and that "software steps" that perform such "software algorithms" cannot produce "a useful tangible and concrete result." Such notions of the Examiner are clearly at odds with the reality of the computer industry and society today in which billions of dollars are expended because execution of such computer instructions in the form of software steps produce real, recognized and demanded results. Such results are not abstract, are not non-repeatable and are not lacking in utility. If execution of computer instructions in the form of software steps were merely abstract or non-repeatable operations lacking in utility, then the huge market for such products would not exist.

20.6. Applicant's claimed method is not abstract, is repeatable and is particularly useful because it permits computer programs written with "legacy instructions" to be executed efficiently as blocks of translated instructions. Typically, the translated instructions execute on more modem computers that may not have even existed when the computer programs with "legacy instructions" were originally written."

6. **Examiner Response:**

Regarding section 20.4, 20.6, Applicants statements amount to nothing more than a conclusionary statement and general allegation that "dynamic emulation of legacy instructions" produces "a useful, tangible, and concrete final result". The final result is "emulation of legacy instructions" and no one can reasonably question that such a result is both "tangible" and "useful"."

Regarding section 20.5, respectfully, the existence of a "huge market" software industry does not make software patentable.

The claimed invention is drawn to software, per se. Which additionally, does not provide a concrete, useful, and tangible final result.

Applicants' arguments have been fully considered but are unpersuasive. Rejection **maintained**.

Response: 35 U.S.C. § 102 Rejection

7. **Background**

Claims 1, 3, 5, and 7 stand rejected under 35 U.S.C. 102(b) as being anticipated by Walters **(US 5,768,593)**.

8. **Applicants argue (section 21.2 to 21.4 of Remarks):**

"21.2. Applicant traverses the rejection under 35 U.S.C. 102(b) for the following reasons.

21.2.1. Applicant's Claim 1 by way of example requires "linking the particular translated blocks" into a particular linked group corresponding to said particular legacy block," said linking using a link in each particular translated block to point to a location of the next particular translated block of the particular linked group" as quoted from Applicant's Claim 1 in Section 21.1.6 above where the Examiner argues that such limitation is found in col: 7 line: 52-63 of Walters '593. However, col: 7 line: 52-63 of Walters '593 does not describe or suggest such a limitation.

[...]

21.2.4. [...] The operation is described in the Examiner's citation col: 7 line: 52-63, particularly, the last four lines thereof as "... the cross-compiler continues with compilation of a block of non-native code (170), and then the resulting native code block is executed (step 172)." Notice in that quotation that native code block is singular. No reference is made to plural Code Blocks" and no reference is made to linking of Code Blocks" anywhere in the Examiner's citation col: 7 line: 52-63.

Furthermore, Applicant cannot find anything else in Walters '593 that in any way teaches the linking of Code Blocks in the Walters '593 Code Cache 118.

[...]

21.3. All of the Claims dependent from Claim 1 are distinguished over Walters '593 in the same manner as Claim 1 and as discussed above in connection with the Examiner's Responses to Applicants Remarks in prior RESPONSE B.

21.4. The Remarks above pertaining to Claim 1 apply equally to Claim 7."

9. **Examiner Response:**

The citations are merely exemplary.

Regarding Section 21.2.4 and Applicant's statement that "no reference is made to plural code blocks", attention is drawn to, among many other examples and instances, **(col: 3 line: 40-41)**, which recites "cross-compiler for converting blocks of non-native code into blocks of native code" (emphasis added). Regarding section 21.2.4, and Applicant's statement that Walters '593 does not in "any way" teach linking of Code Blocks, attention is drawn to, among many other examples and instances, **(col: 5 line: 19-28)**, which discloses converting branch instructions into a sequence of instructions. A sequence is inherently linked such that when the block executes the comparison code and a jump is determined to be appropriate the address to which the jump is pointing to serves as the linkage to the following block. Further, attention is drawn to **(col: 3 line: 58-60)** which discloses that translated native code blocks are executed until an exit instruction is encountered. A branch instruction may be an exit instruction to another block of code, and thus, serve as a link (pointer to another address of another code block).
In view of the above, the rejections are being maintained.

10. **Background:**

Claims 1 and 7 stand rejected under 35 U.S.C. 102(b) as being anticipated by Mann **(US 6,529,862)**.

11. **Applicants argue (section 22.2 of Remarks):**

"22.2.2. Referring to col: 2 line: 44-60 of Mann '593, it states in lines 53 - 56 that:
"Upon completion of the Host code block, execution control is returned to the emulator, with an indication of the next Target system instruction to execute. 22.2.2.1. It is clear from the quote from col: 2 line: 44-60 of Mann '593 that control after one block is always returned to the emulator; it is not linked to another block as in Applicant's claims.
22.2.3. Referring to col: 6 line: 11-28 of Mann '593, it states in the last five lines that:
"Control is then transferred to the Host code 88 at that point. The Host code 88 is then executed until the end of a block is encountered, at which time control is transferred back to the emulator with an indication of where to pick up interpreting code."
22.2.3.1. It is clear from the quote of col" 6 line" 11-28 of Mann '593 that control after one block is always returned to the emulator; it is not linked to another block as in Applicant's claims.

22.2.3.2. Referring to col" 6 line" 47-61) of Mann '593, nothing therein discusses processing at the end of a block. It therefore has no suggestion about exiting one block and directly entering a new block according to a link in the block as in Applicant's claims."

12. **Examiner Response:**

Regarding the above arguments, it is noted that Applicants are arguing features not claimed which are summed up in Remarks section 22.2.3.2. Specifically, the claims do necessitate exiting one block and directly entering a new block. In fact, such language may raise questions of enablement. See paragraph 0026 of the Instant Application's PGPUB Specification, which discloses that control is returned to a "transfer routine" which is called at the end of each RISC block to locate the next block. The "direct" execution is not claimed, and if claimed may result in a 35 U.S.C. § 112 first paragraph enablement rejection. Mann's emulator uses the links at the end of the code to follow to and execute the subsequently linked code blocks. It is quite clear that the "indication of the next Target system instruction to execute" correlates to the link to the following code block to be executed.

In view of the above, the rejections are being maintained.

Claim Rejections - 35 USC § 101

> 35 U.S.C. 101 reads as follows:
> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

13. Claims 1-6 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

> **MPEP 2106 recites, in part:**
> "...USPTO personnel shall review the claim to determine it produces a useful, tangible, and concrete result. In making this determination, the focus is not on whether the steps taken to achieve a particular result are useful, tangible, and concrete, but rather on whether the final result achieved by the claimed invention is "useful, tangible, and concrete." (emphasis added)

13.1 The method claims do not produce a useful, tangible, and concrete final result. The steps of the method claims do not produce a useful, tangible, and concrete final result. They merely recite a software algorithm, *per se*, which, for example, does not display, store, or otherwise provide a useful tangible output. Note exemplary claim 1 which only recites software steps and does not produce a

useful tangible and concrete result. See MPEP 2106. The claimed invention is drawn to software, per se. Which additionally, does not provide a concrete, useful, and tangible final result.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 8-14 are rejected under 35 U.S.C. 112, second paragraph, as being **indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 8, the limitation contains a number of ambiguities which render the claim indefinite:

> organizing the particular translated instructions into one or more particular translated blocks, each translated block including a plurality of contiguous translated instructions stored in a cache,

Specifically, the limitation before the limitation above translates a particular legacy instruction into **one** or more particular translated instructions, and the limitation above states that the translated instructions are translated into translated blocks and each block including a plurality of contiguous translated instructions. This raises an indefiniteness issue. Specifically, it conflicts with the "**one** or more particular translated instructions" limitation.

Additionally, in the limitation quote above it is unclear whether the cache is part of the translated block. Specifically, it is read as each translated block including code stored in a cache. Does this mean that the code is stored in a cache, or does this mean that the cache is included in the translated block.

Clarification is required.

15. Claims not specifically mentioned are rejected by virtue of their dependency.

16. The Applicants are required to fix all other similar occurrences of the above-cited deficiencies.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under

this section made in this Office action:
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claims 1, 3, 5, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Walters **(US 5,768,593)**.

Walters discloses: 1. A computer-implemented method for dynamic emulation of legacy instructions comprising:

accessing said legacy instructions in legacy blocks, each legacy block including a plurality of legacy instructions **(col: 4 line: 4-8 legacy blocks ... "extended block of 'qualifying' non-native code"; col: 4 line: 20-28 instructions ... codes; col: 6 line: 18-26 ... legacy code)**,

for each particular legacy instruction in a particular legacy block,

translating the particular legacy instruction into one or more particular translated instructions for emulating the particular legacy instruction **(col: 7 line: 16-23; col: 7 line: 52-63)**,

organizing the particular translated instructions into one or more particular translated blocks **(col: 7 line: 52-63)**,

linking the particular translated blocks into a particular linked group corresponding to said particular legacy block; said linking using a link in each particular translated block to point to a location of the next particular translated block of the particular linked group **(col: 7 line: 52-63 the entry point serves as a pointer to a next particular block (pre-defined set of non-native instructions))**,

executing the particular translated instructions in the particular translated by executing the linked group translated blocks **(col: 5 line: 19-30; col: 7 line: 52-63)**.

Walters discloses: 3. The method of Claim 1 wherein said particular translated instructions are stored in a cache and wherein said particular translated instructions are purged from said cache only when all said particular translated instructions of particular translated blocks are also purged from said cache **(Fig 3**

item 164 and its description; col: 4 line: 46-57; col: 6 line: 28-29; col: 3 line: 35-44, col: 6 line: 3-10; Cache is not explicitly defined in the specification as such it takes its ordinary meaning in the art: A memory area where frequently accessed data can be stored for rapid access. Source: http://www.orafaq.com/glossary/faqglosc.htm).

Walters discloses: 5. The method of claim 1 wherein said legacy instructions are object code instructions compiled/assembled for a legacy architecture **(col: 1 line: 56 to col: 2 line: 4)**.

As per claim 7, note the rejection of claim 1 above. The Instant Claim recites substantially same limitations as the above-rejected claim and therefore rejected under same prior-art teachings.

18. Claims 1, 7 8, 10, and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Mann **(US 6,529,862)**.

Mann discloses: 1. A computer-implemented method for dynamic emulation of legacy instructions comprising:

accessing said legacy instructions in legacy blocks, each legacy block including a plurality of legacy instructions **(col: 5 line: 64-63)**,

for each particular legacy instruction in a particular legacy block,

translating the particular legacy instruction into one or more particular translated instructions for emulating the particular legacy instruction **(Fig 3, 4, 5, and their descriptions; col: 2 line: 44-60)**,

organizing the particular translated instructions into one or more particular translated blocks **(col: 2 line: 44-60)**,

linking the particular translated blocks into a particular linked group corresponding to said particular legacy block; said linking using a link in each particular translated block to point to a location of the next particular translated block of the particular linked group **(col: 2 line: 44-60; col: 6 line: 11-28; col: 6 line: 47-61)**,

executing the particular translated instructions in the particular translated by executing the linked group translated blocks **(col: 6 line: 11-28)**.

As per claim 7, note the rejection of claim 1 above. The Instant Claim recites substantially same limitations as the above-rejected claim and therefore rejected under same prior-art teachings.

As per claim 8, note the rejection of claim 1 above. The Instant Claim recites substantially same limitations as the above-rejected claim and therefore rejected under same prior-art teachings, but for said logical group including a first translated block, one or more next translated blocks and a last block, said linking using a linked list in said cache including a first link in the first translated block that points to a location in the cache of a next translated block, one or more next links in the next translated blocks where each next link points to a location in the cache of a subsequent one of the next translated blocks, and a last link that points to the last block of the logical group **(col: 6 line: 47-61)**.

As per claim 10, note the rejection of claim 1 above. The Instant Claim recites substantially same limitations as the above-rejected claim and therefore rejected under same prior-art teachings.

As per claims 12-14, note the rejection of claims 4-6 above. The Instant Claims recite substantially same limitations as the above-rejected claims and therefore rejected under same prior-art teachings.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters **(US 5,768,593)** as applied to claim 1 above, and further in view of Scalzi **(US 5,540,013)**.

As per claim 4, Walters discloses all limitations of claim 1. Walters, although enabled to use the invention for S/390 architecture, does not explicitly disclose using such architecture in the emulation of the legacy system **(col: 1 line: 40-44)**. Scalzi however discloses an analogous emulation system having the said feature **(col: 17 line: 54-67)**. It would have been obvious to one of ordinary skill in the art <hardware emulation / software emulation / PowerPC emulation / virtual machines / etc> at the time of Applicant's invention. The motivation is given by the primary reference in **(col: 1 line: 40-44, col: 1 line: 18-25**

... IBM PC compatible computers), i.e. in order to use the programs developed for one system on another system without having to re-design and re-development the programs; thus, saving cost, time and effort.

As per claim 6, Walters discloses all limitations of claim 1. Walters is enabled such that translated instructions are for execution in a RISC architecture. Walters however does not explicitly disclose such a feature. Scalzi however discloses an analogous emulation system having the said feature **(col: 2 line: 3-23)**. It would have been obvious to one of ordinary skill in the art <hardware emulation / software emulation / PowerPC emulation / virtual machines / etc> at the time of Applicant's invention. The motivation is given by the primary reference in **(col: 1 line: 40-44, col: 1 line: 18-25 ... IBM PC compatible computers)**, i.e. in order to use the programs developed for one system on another system without having to re-design and re-development the programs; thus, saving cost, time and effort.

20. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann **(US 6,529,862)** as applied to claim 8 above, and further in view of Walters **(US 5,768,593)**.

As per claim 9, Mann discloses all limitations of claim 8. Mann however does not expressly disclose said plurality of contiguous legacy instructions in the legacy block include one or more legacy branch instructions, where the translating step translates the legacy branch instructions to translated branch instructions, where the executing step executes said translated branch instructions and when a taken branch results in a branch target instruction within the logical group, the executing step directly executes the branch target instruction without requiring an external reference to look-up the location of the branch target instruction. Walters however discloses the said features **(col: 12 line: 10-32)**. It would have been obvious to one of ordinary skill in the art <computer engineering / emulation engineering / address translation> at the time of Applicant's invention to combine the references in order to reduce the time required to perform an address look up; thus, generating a faster emulator and saving time and costs associated therewith.

As per claim 11, Mann discloses all limitations of claim 8. Mann however does not expressly disclose where each legacy block has a number of translated blocks where the number of translated blocks differs for different legacy blocks. Walters however teaches the said feature **(col: 13 line: 43-53)**.

Specifically, the non-native instructions are non-native branch conditions which are translated into native branch instructions of varying lengths (minimum number of native code instructions used to handle non-native condition codes vary depending on the type of branch instructions). It would have been obvious to one of ordinary skill in the art <computer engineering / emulation engineering / address translation> at the time of Applicant's invention to combine the references in order to reduce the time required to perform an address look up; thus, generating a faster emulator and saving time and costs associated therewith.

Examiner Notes

21. Applicant is thanked for the exceptionally well-organized Response to Office Action.

Conclusion

22. All claims are rejected.

23. The Instant Application is not currently in condition for allowance.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action (35 U.S.C. § 112 second paragraph rejections). Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Silver whose telephone number is (571) 272-8634. The examiner can normally be reached on Monday thru Friday, 10am to 6:30pm. If attempts to reach the examiner by telephone are

unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER